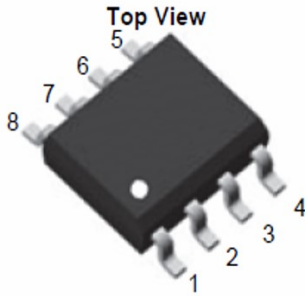
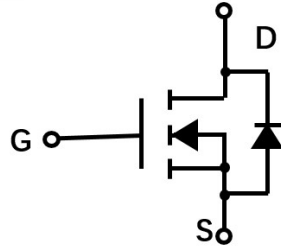
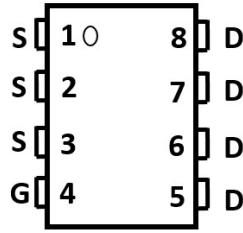


## N-Channel Enhancement Mode Field Effect Transistor



**SOP-8**



### Product Summary

- $V_{DS}$  40 V
- $I_D$  10 A
- $R_{DS(ON)}$  (at  $V_{GS} = 10V$ ) < 15mohm
- $R_{DS(ON)}$  (at  $V_{GS} = 4.5V$ ) < 24mohm

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ\text{C}$	$I_D$	10	A
	$T_A=100^\circ\text{C}$		7.0	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	50	A
Single Pulse Avalanche Energy <sup>B</sup>		$E_{AS}$	70	mJ
Total Power Dissipation	$T_A=25^\circ\text{C}$	$P_D$	3.0	W
	$T_A=100^\circ\text{C}$		1.2	
Thermal Resistance Junction-to-Lead <sup>C</sup>		$R_{\theta JL}$	30	$^\circ\text{C}/\text{W}$
		$R_{\theta JA}$	41.5	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS10N04A	F2	Q10N04	4000	8000	64000	13" reel



# YJS10N04A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =8.0A		12.5	15	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =4.0A		15.5	24	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =10A, V <sub>GS</sub> =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				10	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHZ		917		pF
Output Capacitance	C <sub>oss</sub>			128		
Reverse Transfer Capacitance	C <sub>rss</sub>			108		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		23.6		nC
Gate-Source Charge	Q <sub>gs</sub>			4.4		
Gate-Drain Charge	Q <sub>gd</sub>			6.3		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us		0.4		
Reverse Recovery Time	t <sub>rr</sub>			7		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =2A, R <sub>L</sub> =1Ω R <sub>GEN</sub> =3Ω		10		ns
Turn-on Rise Time	t <sub>r</sub>			56		
Turn-off Delay Time	t <sub>D(off)</sub>			27		
Turn-off fall Time	t <sub>f</sub>			72		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJL</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## ■ Typical Performance Characteristics

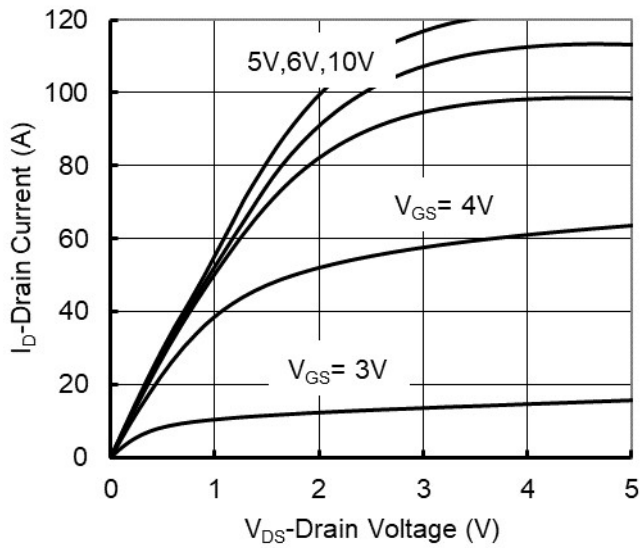


Figure 1. Output Characteristics

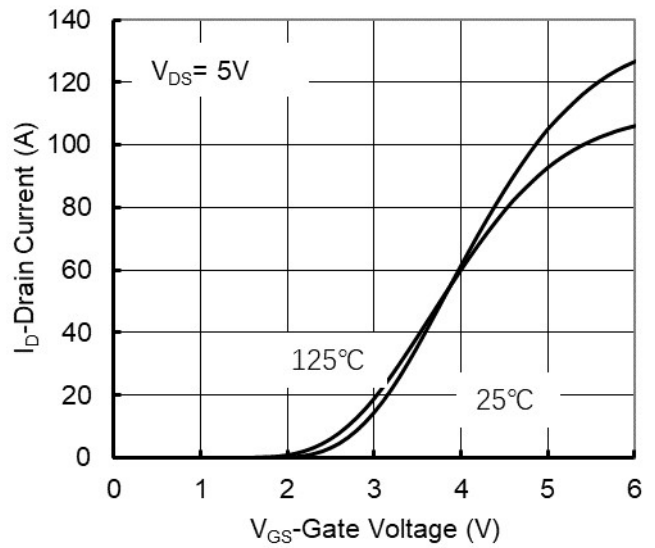


Figure 2. Transfer Characteristics

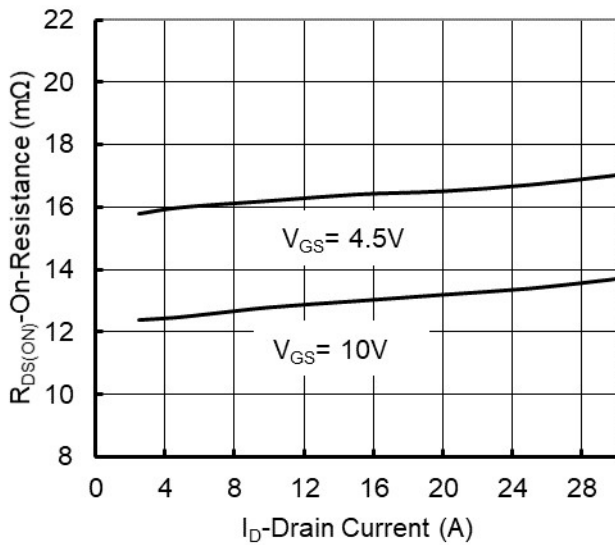


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

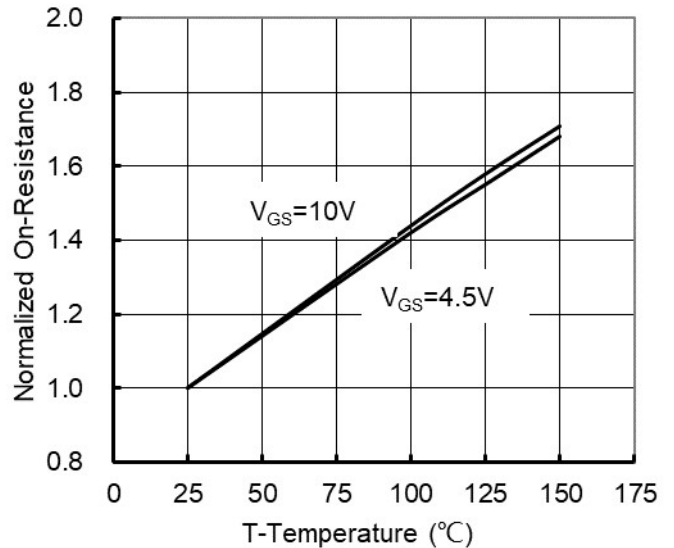


Figure 4. On-Resistance vs. Junction Temperature

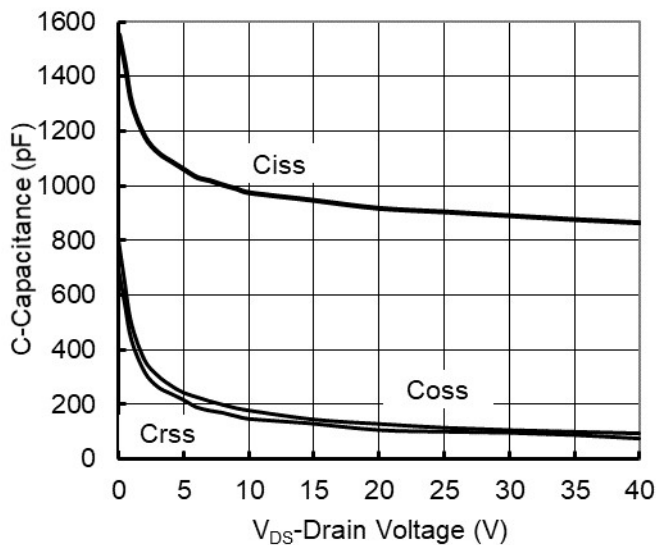


Figure 5. Capacitance Characteristics

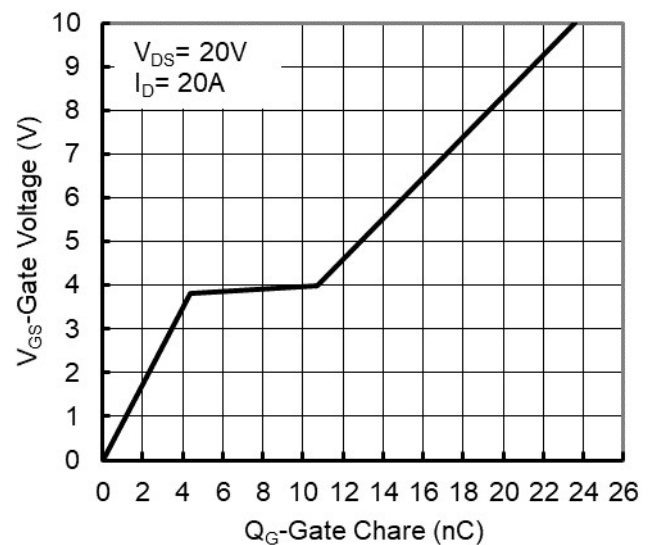


Figure 6. Gate Charge



# YJS10N04A

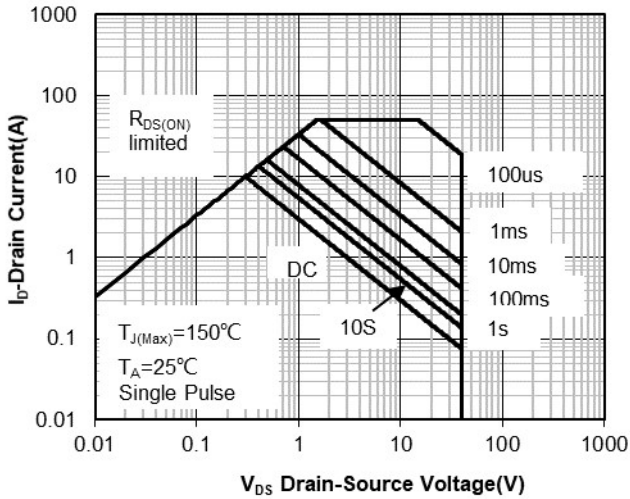


Figure 7. Safe Operation Area

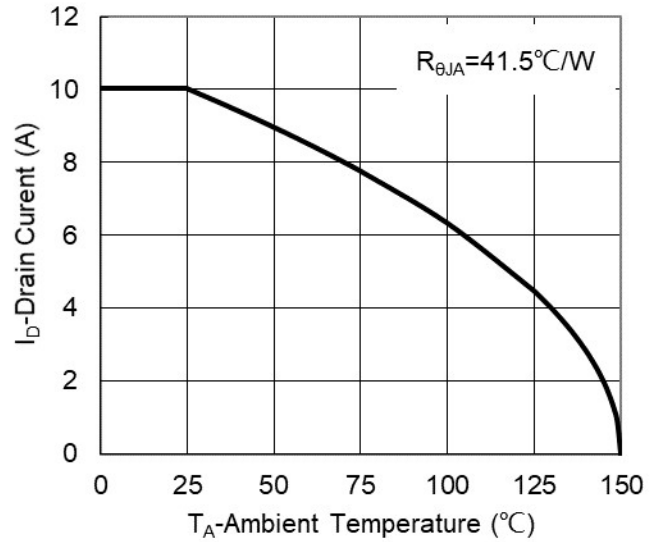


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

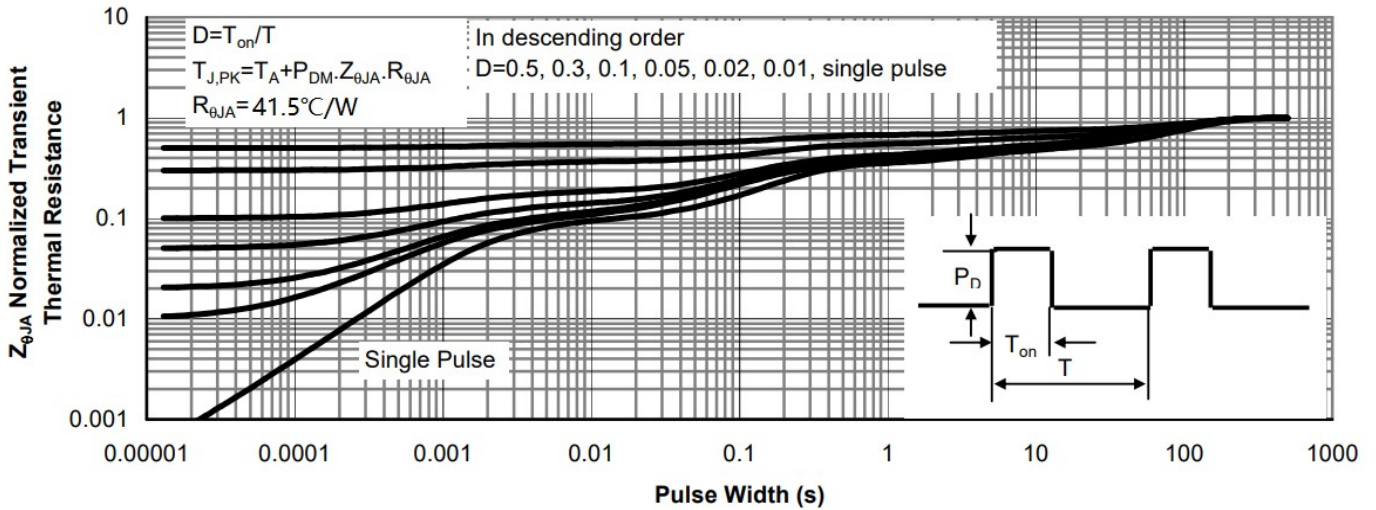
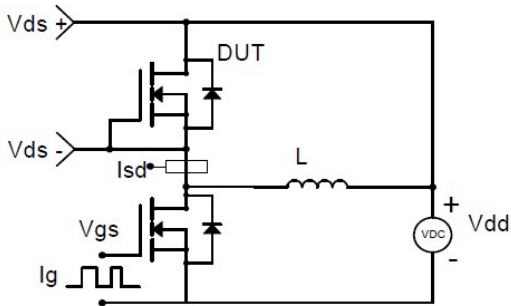


Figure 9. Normalized Maximum Transient Thermal Impedance



**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

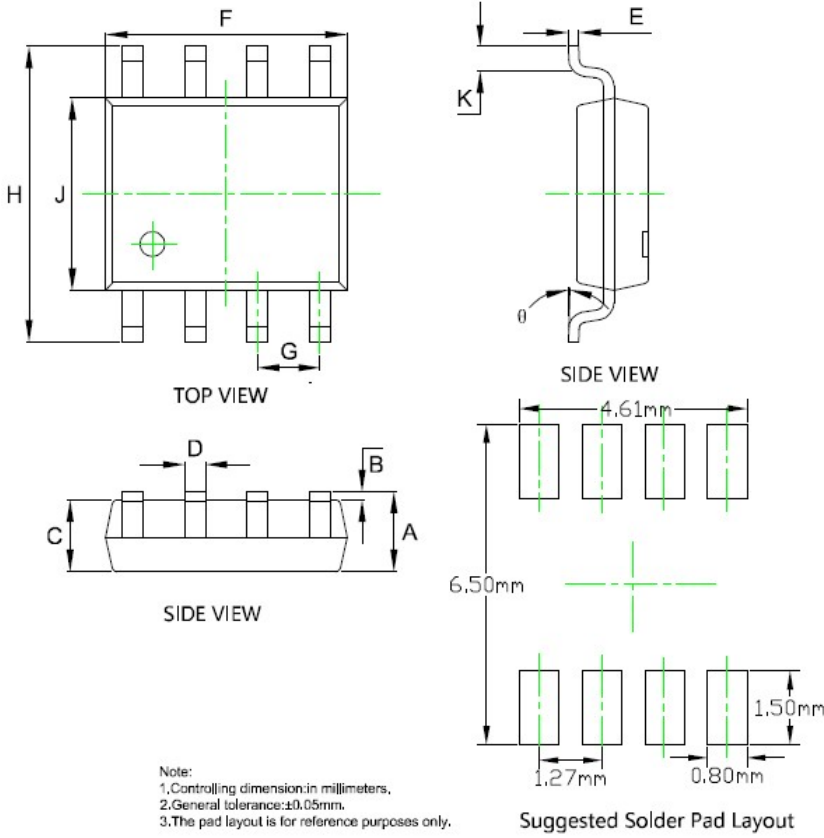


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJS10N04A

## ■ SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°



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